

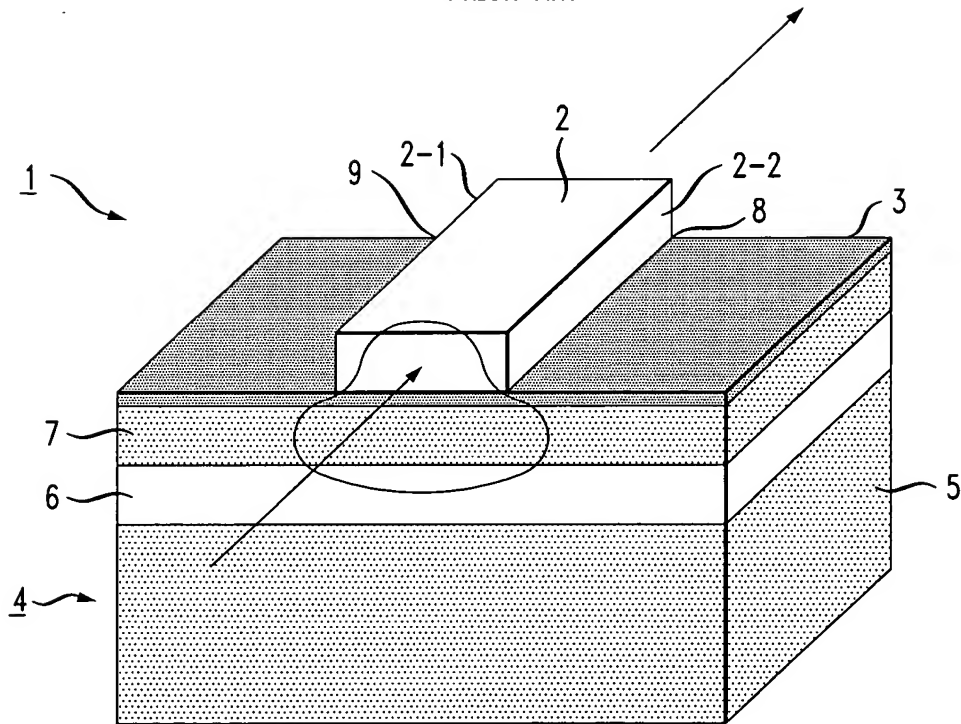


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FIG. 1

PRIOR ART



A cross-sectional view of a semiconductor device 4. The device is built on a substrate 6. A gate stack 10 is formed on the substrate, consisting of a gate dielectric 14 and a gate electrode 16. A source/drain region 11 is formed in the substrate, containing a dopant 12. A channel region 13 is formed in the substrate, containing a dopant 15. A gate electrode 18 is formed on the gate stack 10, and a gate electrode 19 is formed on the gate stack 10. A gate electrode 13 is formed on the gate stack 10, and a gate electrode 15 is formed on the gate stack 10. A gate electrode 11 is formed on the gate stack 10, and a gate electrode 12 is formed on the gate stack 10.

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FIG. 6

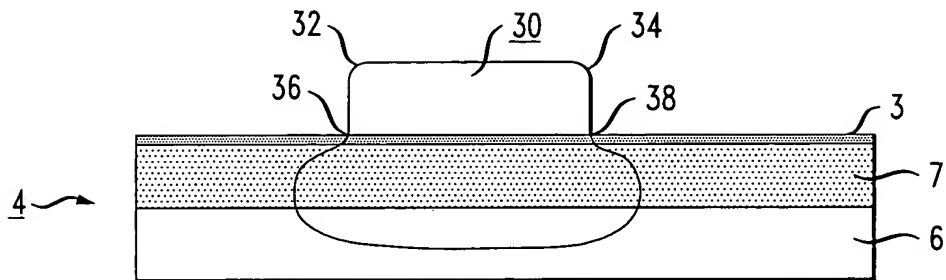
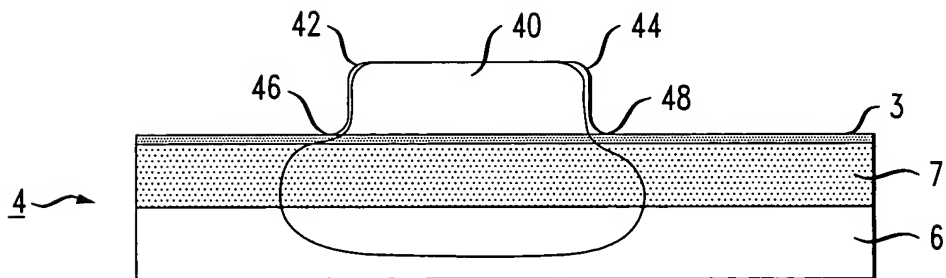


FIG. 7



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FIG. 8

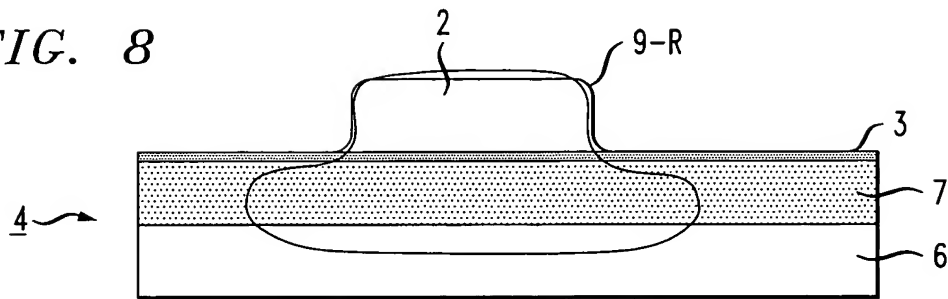


FIG. 9

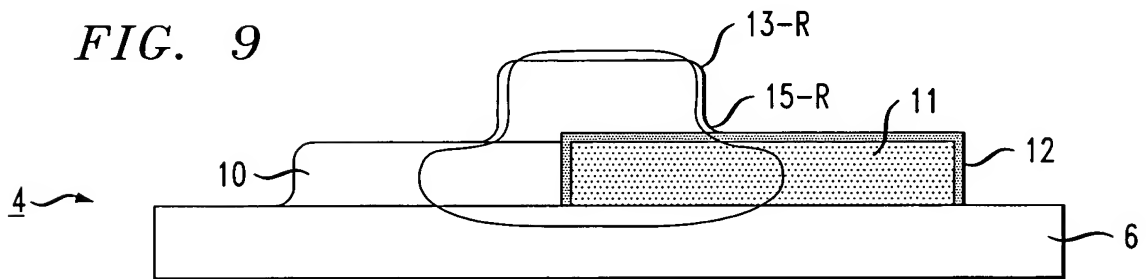


FIG. 10

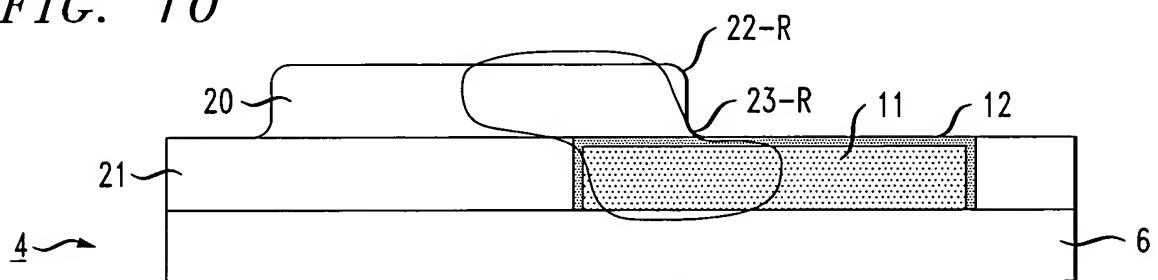
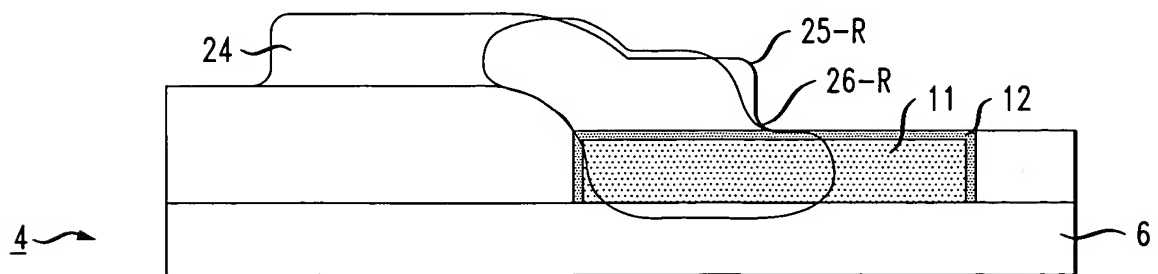


FIG. 11



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FIG. 12

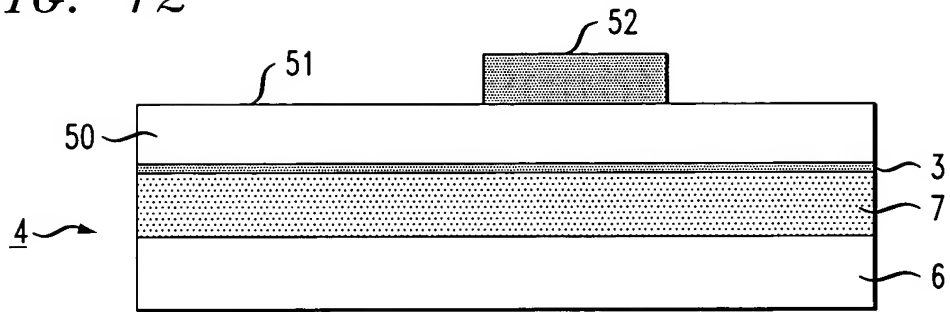


FIG. 13

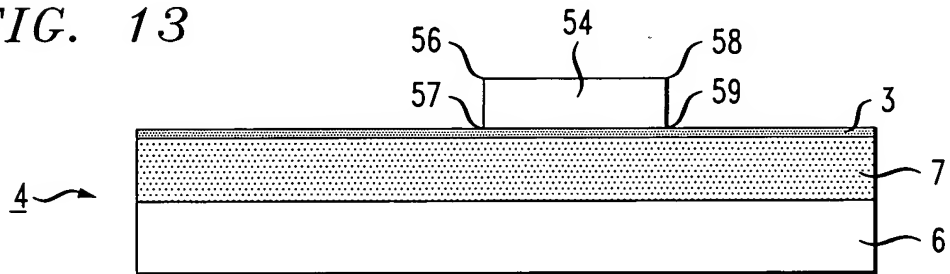


FIG. 14

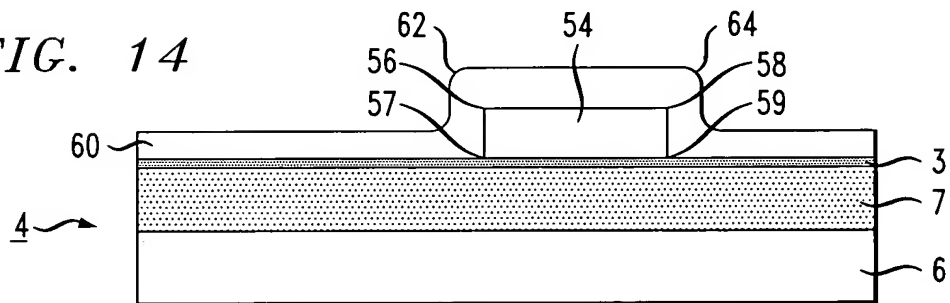
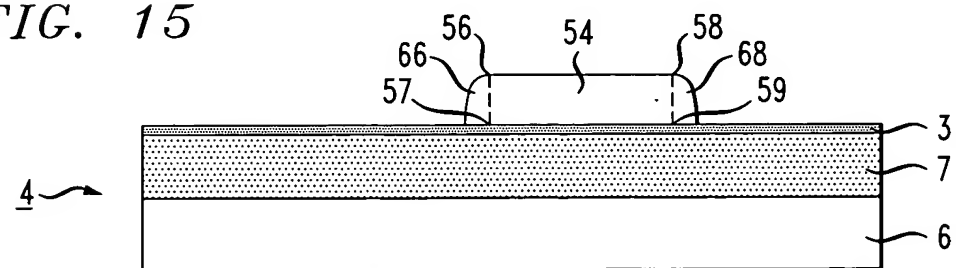


FIG. 15



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FIG. 16

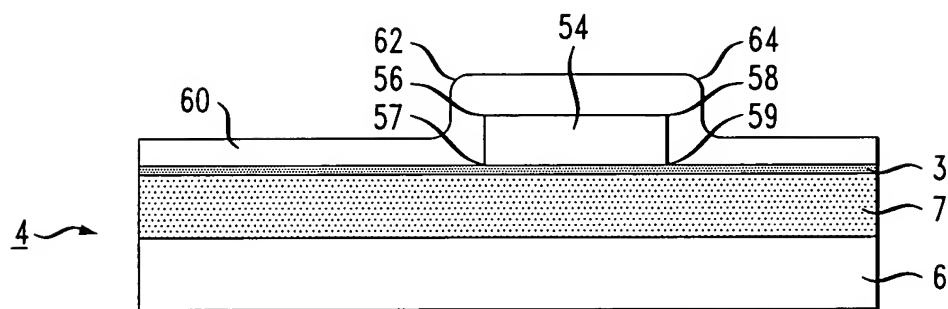


FIG. 17

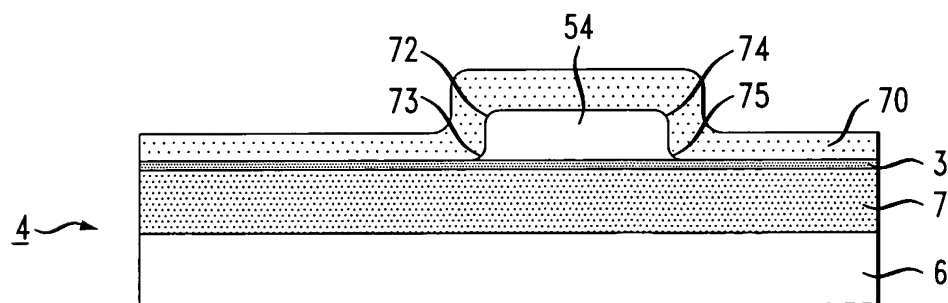


FIG. 18

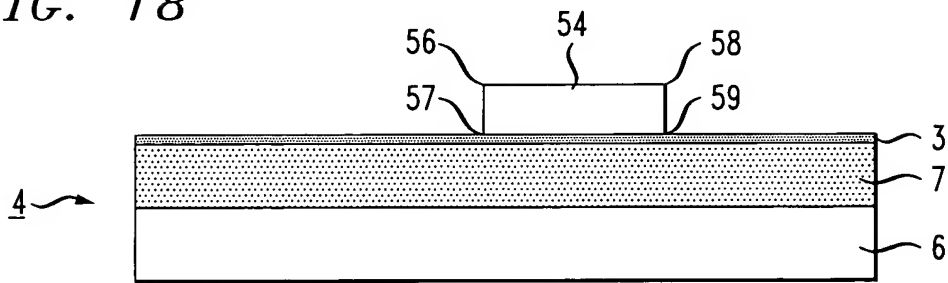


FIG. 19

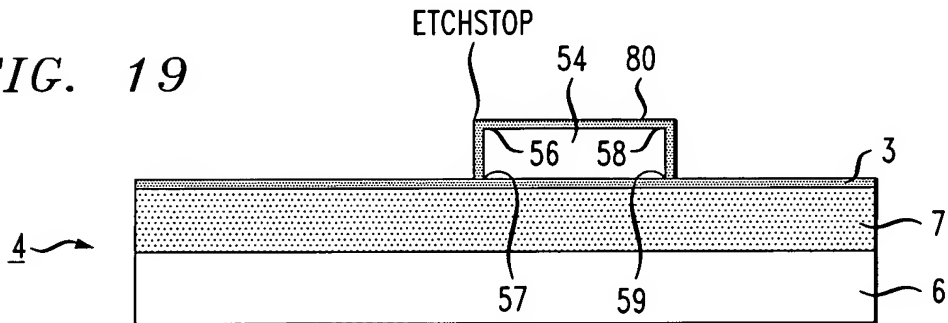


FIG. 20

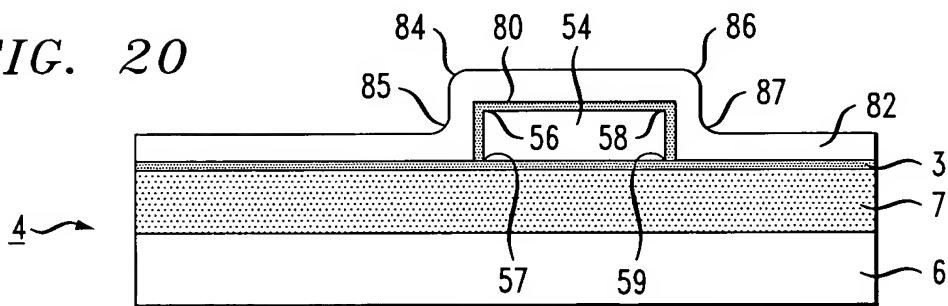
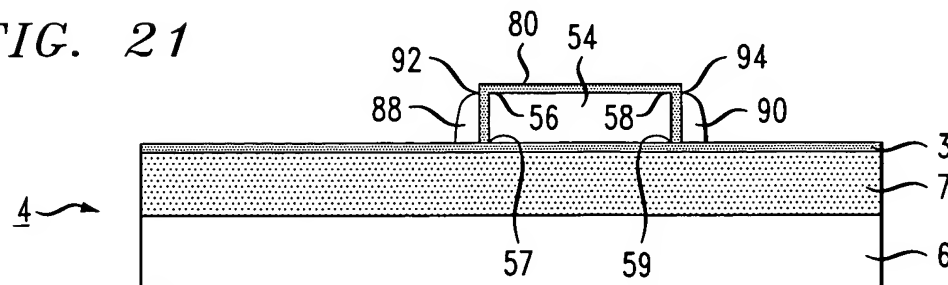


FIG. 21



This cross-sectional view shows a trench structure formed in a substrate. The substrate consists of a top layer (3), a middle layer (7), and a bottom layer (6). A trench (54) is formed in the top layer (3), with its bottom surface (56) and side walls (58) exposed. The trench is filled with a material (57). The top surface of the trench is covered by a layer (96). The side walls of the trench are covered by a layer (98). The bottom surface of the trench is covered by a layer (91). The top surface of the substrate is covered by a layer (89). A reference numeral 4 with an arrow points to the right.

[illegible]

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FIG. 24

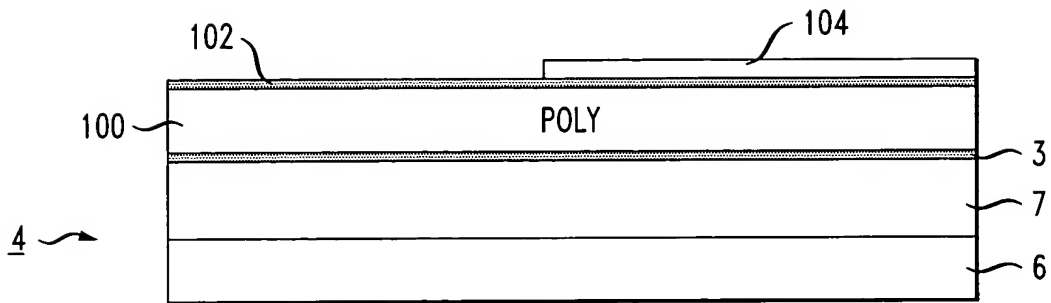


FIG. 25

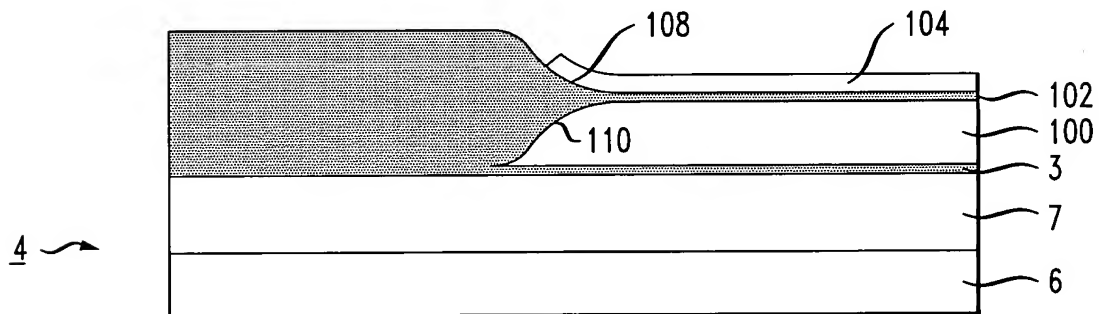
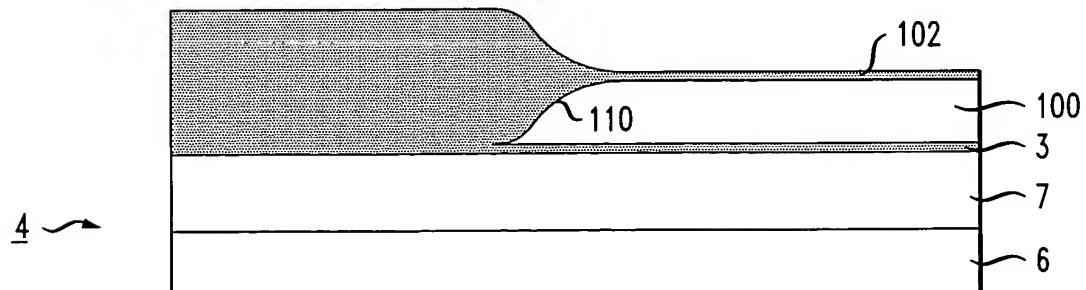


FIG. 26



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FIG. 27

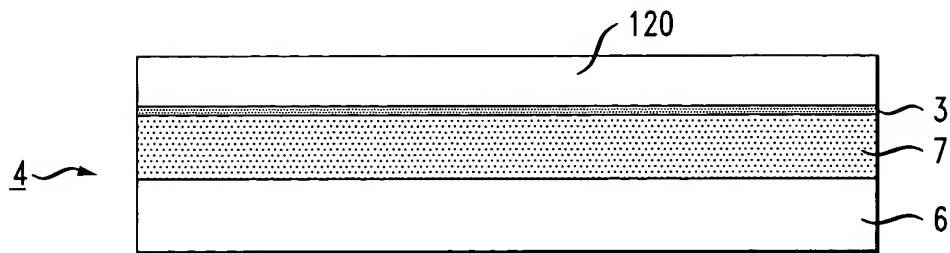


FIG. 28

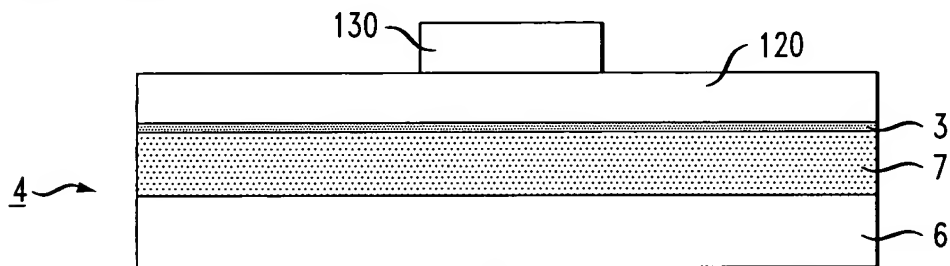


FIG. 29

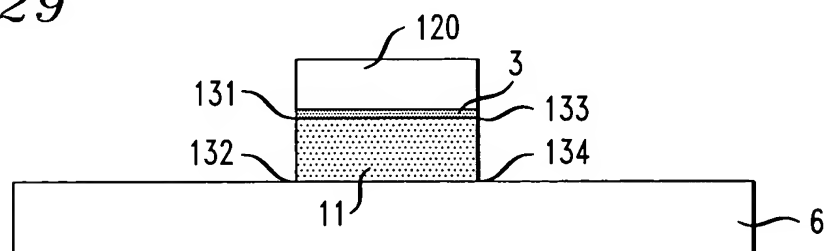
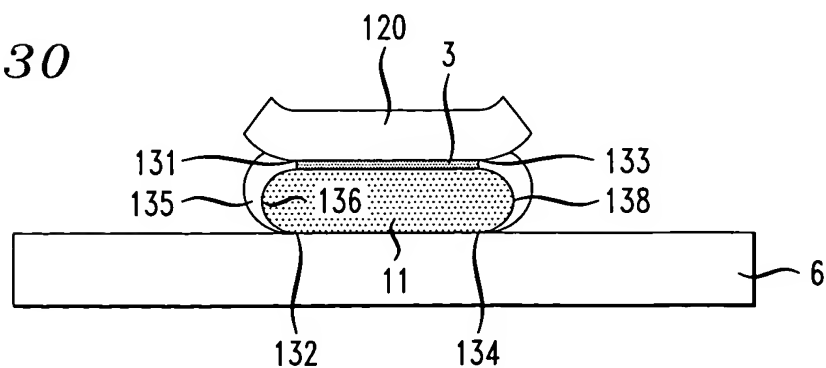


FIG. 30



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FIG. 31

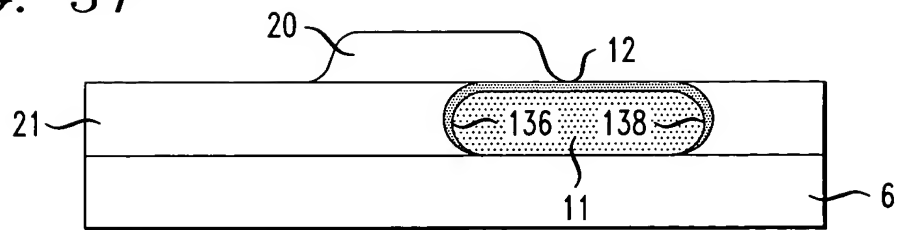


FIG. 32

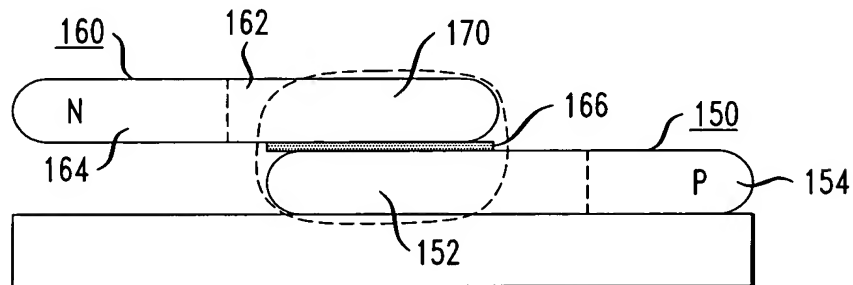


FIG. 33

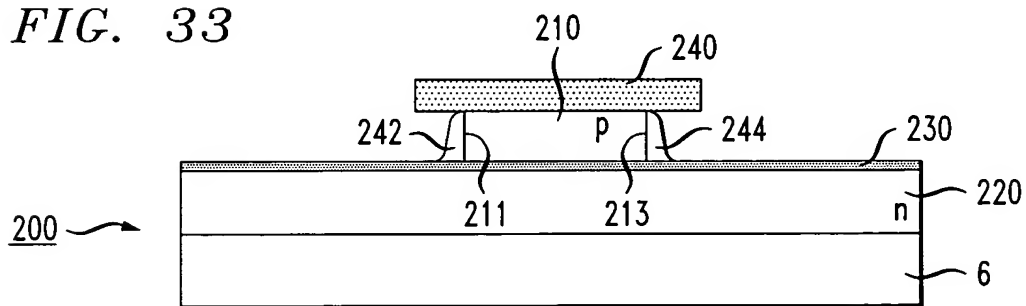


FIG. 34

